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# 3D Free-Form Patterning of Silicon by Ion Implantation, Silicon Deposition, and Selective Silicon Etching

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**A method for additive layer-by-layer fabrication of arbitrarily shaped 3D silicon micro- and nanostructures is reported. The fabrication is based on alternating steps of chemical vapor deposition of silicon and local implantation of gallium ions by focused ion beam (FIB) writing. In a final step, the defined 3D structures are formed by etching the silicon in potassium hydroxide (KOH), in which the local ion implantation provides the etching selectivity. The method is demonstrated by fabricating 3D structures made of two and three silicon layers, including suspended beams that are 40 nm thick, 500 nm wide, and 4 μm long, and patterned lines that are 33 nm wide.**

## 1. Introduction

Silicon (Si) is one of the most attractive materials for many micro- and nanoscale devices, due to its excellent mechanical, optical, and electrical properties.[1] Conventional Si machining techniques, including lithography and deep Si etching, allow cost-efficient implementation of simple suspended three dimensional (3D) Si structures. However, more complex 3D Si structures can only be implemented by using complicated fabrication schemes involving a multitude of different processes. Additive layer-by-layer manufacturing techniques for polymer and metal 3D structures are well established. In these techniques, the arbitrarily shaped 3D structures are formed by stacking patterned material layers on top of each other.[2–10] A comparable process that allows additive layer-by-layer fabrication of 3D Si structures could provide a wealth of opportunities for new types of nanophotonics, nano-electromechanical systems (NEMS) and micro-electromechanical systems (MEMS).

Existing additive layer-by-layer manufacturing techniques include stereolithography,[2,3] solid ground curing,[2] selective laser sintering,[2,7] 3D inkjet printing,[2] fused deposition modeling,[2,8–18] and laminated object modeling.[2,19,20] In stereolithography, solid ground curing, and direct laser writing, 3D polymer structures are fabricated by locally exposing a photosensitive polymer with light, which allows subsequent selective dissolution of the polymer.[2–6] In 3D inkjet printing, and in some fused deposition modeling techniques, 3D structures are formed by printing functional inks, often in combination with supporting sacrificial inks that are subsequently selectively dissolved.[2,8] Typical materials used in these techniques include polymers, waxes, and inks filled with e.g. metal, carbon, or ceramics. Laser-beam,[11–13] focused ion-beam (FIB),[14–16] electron-beam,[14] and proton-beam[17,18] assisted deposition are other fused deposition modeling techniques for additive fabrication of 3D structures. Laser-assisted deposition has been demonstrated for the fabrication of 3D Si structures with dimensions in the range of tens of μm.[12,13] Focused ion-beam, electron-beam, and proton-beam assisted deposition methods can achieve structural dimensions of the order of a few tens of nm, but the fabrication of suspended Si structures has not been shown with these techniques. Layer-by-layer fabrication of 3D polycrystalline Si structures with dimensions below 1 μm has been demonstrated using conventional semiconductor manufacturing processes.[19,21] The applied processes are combinations of poly-crystalline Si deposition, $SiO_2$ deposition, photolithography, reactive ion etching, chemical-mechanical polishing (CMP), and selective etching of the sacrificial layer. These approaches require a large number of different process and photolithography steps that cannot be easily automated. Transfer printing of pre-patterned Si membranes (laminated object modeling) has been used to fabricate 3D Si structures with dimensions in the micrometer-range.[20,22] It is however difficult to efficiently automate these processes, and to achieve sub-micrometer alignment accuracies during lamination of the pre-patterned membranes.

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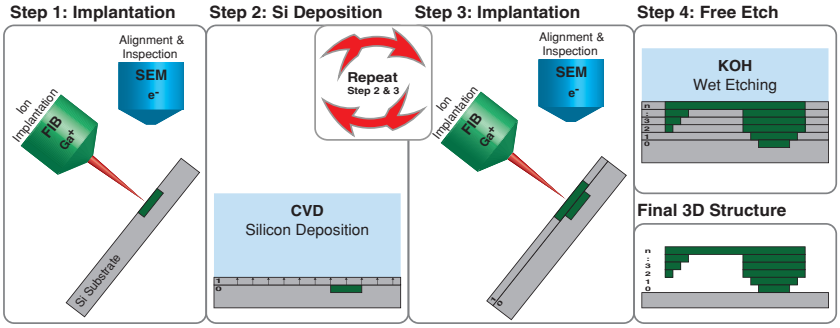


**Figure 1.** A schematic of the additive layer-by-layer fabrication process: Step 1: Local implantation of $Ga^+$ ions into a Si substrate surface using FIB writing. Step 2: CVD of a thin Si layer. Step 3: Local implantation of $Ga^+$ ions in the deposited Si layer using FIB writing. Steps 2 and 3 are repeated until the 3D structure is defined in the Si layers by the locally implanted $Ga^+$ ions. Step 4: Selective etching of the Si that contains no implanted Ga ions in KOH, to obtain the final 3D Si structure.

Here, we report a straightforward method for additive layer-by-layer fabrication of arbitrarily shaped 3D Si micro- and nanostructures. The method is schematically illustrated in **Figure 1**, and consists of a cyclic process of defining a pattern with implanted gallium ions ($Ga^+$) in a Si layer using FIB writing (Figure 1, Steps 1 and 3), followed by chemical vapor deposition of a 40–70 nm thick Si layer (Figure 1, Step 2). By repeating Steps 2 and 3, 3D structures are defined within the deposited Si layers. The local implantation of $Ga^+$ ions into Si results in an etch selectivity for potassium hydroxide (KOH) wet etching,[23–28] tetramethylammonium hydroxide (TMAH) wet etching,[29] and cryogenic reactive ion etching.[30–32] Etch selectivities of >1000 in KOH[28] and >2000 in TMAH[29] have been demonstrated. Thus, the defined 3D Si structures can be formed by selective free-etching, using one of these etches as a final patterning step (Figure 1, Step 4). In this work, free-etching in KOH was used. We demonstrate the feasibility of our method by fabricating 2- and 3-layer 3D structures, including suspended Si beams that are 40 nm thick, 500 nm wide, and up to 4 µm long. To the best of our knowledge, this is the first demonstration of patterning 3D Si structures by additive layer-by-layer fabrication using a cyclic process combining chemical vapor deposition (CVD) of Si layers and local ion implantation by FIB writing with a final etch to form 3D Si structures. The process combines two mature and established fabrication methods: CVD, providing high-quality thin Si layers, and FIB implantation of $Ga^+$ ions in Si, capable of forming patterns with lateral dimensions of below 20 nm and typical implantation depths of 30–50 nm.[26] An important feature of the proposed additive layer-by-layer fabrication process is that it may be possible to implement Si CVD and FIB writing as switched processes in a single automated tool. Such a tool could enable "printing" of 3D Si micro- and nanostructures directly from 3D CAD models, without requiring a fully equipped semiconductor clean-room. To increase throughput, highly parallel FIB writing with multi-ion-beam arrays may even be viable.[33]

## 2. Results and Discussion

To demonstrate the method, both 2- and 3-layer 3D Si structures were fabricated. The 2-layer structures, shown in the scanning electron microscope (SEM) image in **Figure 2**a, have been fabricated by two $Ga^+$ ion implantation steps (10 pC/µm$^2$ dose) and one Si deposition step. The structures consist of four raised Si platforms, with cantilevers extending out from the platforms and doubly clamped Si beams that connect the platforms. In the experiments, the platforms were defined in a (100) Si substrate (p-type, 0.005–0.020 Ω-cm) by $Ga^+$ ion implantation (Figure 1, Step 1). Thereafter, a layer of Si was grown on the wafer at a temperature of 635 °C (Figure 1, Step 2). Next, the beams were defined in the deposited Si layer by a second $Ga^+$ ion implantation (Figure 1, Step 3), followed by a 30 s rapid thermal anneal at 650 °C in an argon atmosphere. Finally, the non-implanted Si was selectively etched in a 30% solution of KOH for 8 min at 36 °C (Figure 1, Step 4). The resulting suspended beams have a width of 500 nm, a thickness of 40 nm, and a length of up to 4 µm. Indicated in Figure 2a are the enlarged areas shown in Figure 2b,d, the line height profiles of Figure 2e,f, and the cross section of **Figure 3**. Figure 2b is an enlarged view of two cantilever beams. The narrower beam is 500 nm wide, and the wider one 2 µm wide. The KOH has freed the narrow beam, while the wide beam is still supported. Given the high selectivity of the KOH etch (>1000), the wide beam could be freed by extending the etch time. The beams show no signs of stress, and are flat after the free-etch. Figure 2c shows the height profile of the complete structure, as measured by white light interferometry. Figure 2d is an

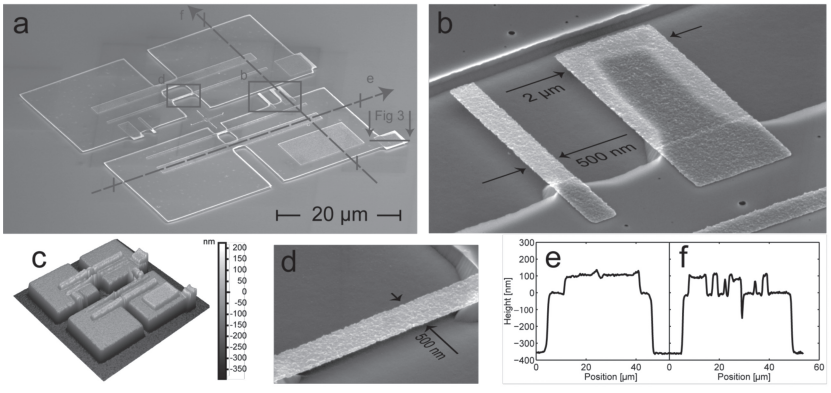


**Figure 2.** a) An SEM image of the fabricated 2-layer structures. Indicated in the image are the enlarged areas shown in (b,d), the line height profiles of (e,f), and the cross section used in Figure 3. b) An enlarged view of two cantilever beams. It is visible that the narrow beam is free-etched while the wide beam is still supported. c) The height profile of the complete structure, as measured with white light interferometry. d) An enlarged view of a doubly clamped beam. e) Height profile along a doubly clamped beam. f) Height profile along a cantilever beam.

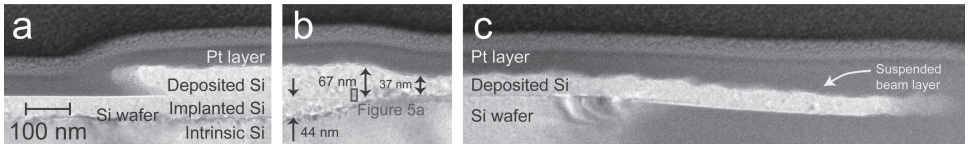


**Figure 3.** TEM cross sections at: a) the edge of the deposited and implanted beam layer; b) the edge of platform implantation. Indicated are the layer thicknesses and the area enlarged in Figure 5a; and c) the suspended deposited and implanted beam layer.

enlarged view of one of the free-etched doubly clamped beams of 500 nm width. The top surface of the patterned Si structures was profiled using atomic force microscopy (AFM). The root mean square (RMS) roughness of the measured $3 \times 3$ μm$^2$ areas was 5.1 nm, which is sufficiently flat for many MEMS, NEMS, and optical applications.

Figure 3 shows a transmission electron microscope (TEM) image of the layer stack along the cross-section indicated in Figure 2a. The three Si layers visible in Figure 3a are, from bottom to top, the intrinsic Si of the substrate, the implanted platform layer, and the grown and implanted beam layer. The platinum (Pt) protective layer was deposited locally via a combination of electron beam and ion beam induced deposition, during the TEM lamella preparation. By comparing, in Figure 3a, the surface level of the implanted platform region on the left to the level of the original wafer surface protected under the deposited layer on the right, we find that no more than a few nm of implanted silicon is removed during the KOH etch. Considering that 350 nm of non-implanted silicon is removed in the same etch step, we observe an etch selectivity in our process of at least the order of 100 between implanted and non-implanted regions. A slight under-etch of the deposited Si layer is visible, most likely due to incomplete penetration of the $Ga^+$ ions through the layer. Figure 3b shows the cross-section at the edge of the platform implantation into the substrate. The thickness of the implanted layer in the platform area is 44 nm. The thickness of the layer deposited over the implanted platform region is 67 nm, and the thickness of the free-etched suspended layer deposited over the non-implanted region is 37 nm. The thickness of the free-etched suspended layer agrees reasonably well with the predictions of the TRIM simulation code.[34] A simulated 30 keV $Ga^+$ ion implantation into Si yields a mean implantation depth of 28 nm, and one standard deviation of ion distribution of 10 nm. For an implanted $Ga^+$ ion area dose of 10 pC/μm$^2$ ($6 \times 10^{15}$ cm$^{-2}$), the thickness of the layer receiving a volume dose above the critical value for achieving an etch selectivity in KOH ($2.2 \times 10^{19}$ cm$^{-3}$)[27] is 60 nm. **Figure 4** shows the simulated implantation profile. The reason for the thinner than expected observed layer could be that diffusion of $Ga^+$ ions during annealing tends to dilute the ion concentration below the critical level in the interface facing non-implanted Si. The difference in thickness of the Si layer grown on implanted and non-implanted Si is the result of a difference in Si growth mechanism on the two regions. This effect is known from so called differential epitaxy, where the growth rates over different types of exposed surfaces vary significantly under identical conditions (gas flow, partial pressure, temperature), i.e., faster growth might occur on implanted regions as compared to non-implanted regions, where the surface is perfectly

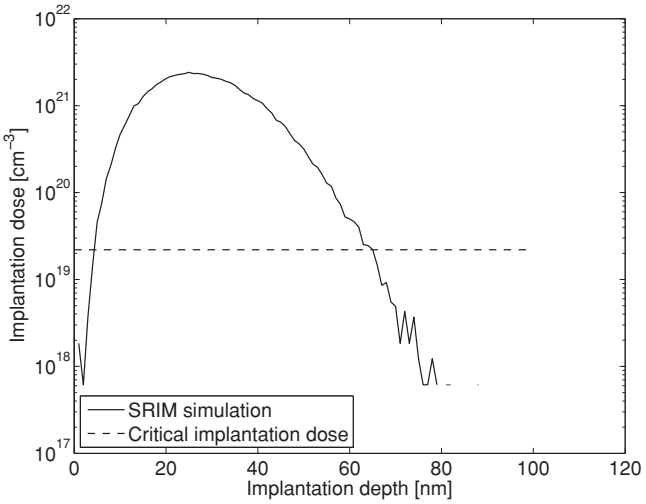


**Figure 4.** The volume dose profile of a 30 keV $Ga^+$ ion implantation into Si at an area dose of 10 pC/μm$^2$ ($6 \times 10^{15}$ cm$^{-2}$), calculated with the TRIM simulation code.[34] The mean implantation depth is 28 nm, the standard deviation of ion distribution is 10 nm, and the dose is above the critical value for etch selectivity in KOH, which is $2.2 \times 10^{19}$ cm$^{-3}$, in a 60 nm thick layer.

crystalline.[35,36] The gray rectangle in Figure 3b indicates the area enlarged in **Figure 5**a. Figure 3c shows the suspended beam layer embedded in the platinum cover layer. Figure 5a shows a high-resolution TEM image of the area indicated in Figure 3b, i.e., around the original wafer surface (shown in more detail in Figure 5b). Lattice fringes are clearly visible, indicating that both the implanted layer of the wafer and the deposited layer are polycrystalline with grains smaller than 10 nm. This is confirmed by the fast Fourier transform (FFT) analysis shown in Figure 5c. Amorphization of Si is a known result of FIB $Ga^+$ ion implantation,[37] and the subsequent annealing steps have caused re-crystallization of the amorphized Si to a polycrystalline state.

To demonstrate the feasibility of our fabrication method for multilayer 3D structures with more than one deposited Si layer, 3-layer structures have been fabricated. The 3-layer structures shown in **Figure 6**a were fabricated by three implantation steps and two Si deposition steps. The base substrate was a (100) Si substrate (p-type, 14–22 Ω cm) and the first layer was patterned in the Si substrate. Thereafter, two Si deposition steps with subsequent FIB implantation steps were performed. The same process sequence and parameters as for the 2-layer structures were used for the 3-layer structures, including wafer cleaning, rapid thermal anneals, FIB implantations, Si layer depositions,

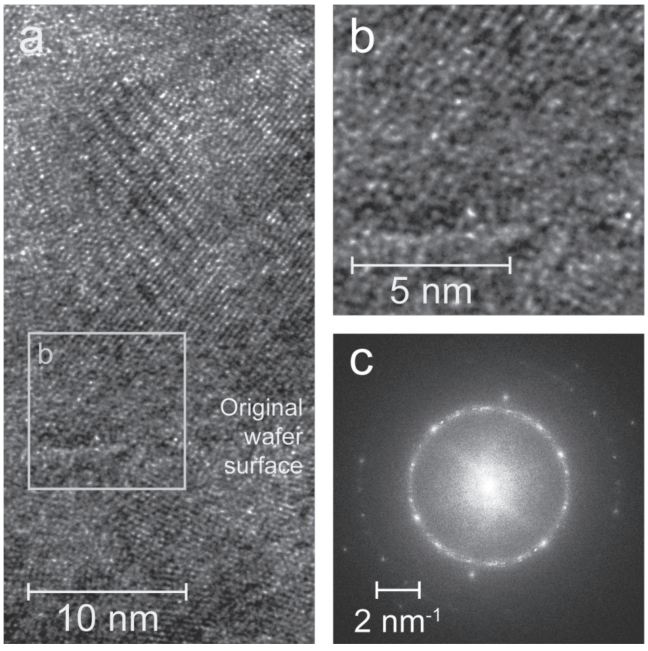


**Figure 5.** a) A TEM image of the cross section of the layer stack at the edge of the platform implantation. b) An enlarged view of the interface between the original wafer surface and the deposited and implanted layer. c) FFT analysis of (a).

and the final KOH etch. The structures demonstrate all the different overlaps possible with three layers. To investigate the limits of the smallest feature size that can be implemented, resolution test structures with narrow line patterns were written in a deposited layer using the same procedure. Figure 6b shows the narrowest patterned Si lines that were resolved, which are as narrow as 33 nm. The sloped sidewalls that can be seen beneath the lines are indicative of preferential etching in different lattice directions, which is characteristic of KOH etching. The results from the resolution test structures clearly demonstrate the potential of this method for fabricating 3D Si devices with dimensions on the nm-scale.

## 3. Conclusions

A simple additive layer-by-layer method for the fabrication of arbitrarily shaped 3D Si micro- and nanostructures is reported.

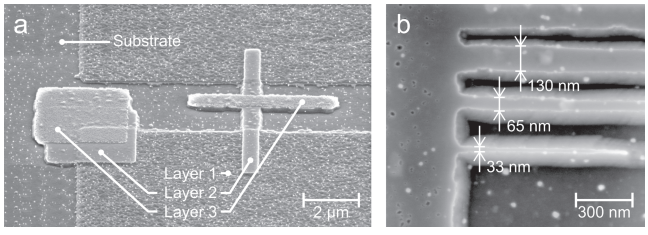


**Figure 6.** a) An SEM image of 3-layer structures. b) An SEM image of lines of widths as small as 33 nm, patterned in a deposited layer.

The feasibility of the method is demonstrated by fabricating suspended Si beams with sub-micrometer dimensions, and patterned lines with dimensions on the nanometer scale, in 2- and 3-layer processes. It may be possible to implement Si CVD and FIB writing as switched processes in a single automated tool, which could enable "printing" of 3D Si micro- and nanostructures directly from 3D CAD models. Thus, the proposed technology could change and greatly simplify the fabrication of many MEMS, NEMS and Si photonic devices, without requiring a fully equipped semiconductor cleanroom. This layer-by-layer fabrication method is in principle also viable for the implementation of 3D structures in semiconductors other than Si.

## 4. Experimental Section

In the FIB implantation, an area dose of 10 pC/µm$^2$ ($6 \times 10^{15}$ cm$^{-2}$) of $Ga^+$ ions was used, at an acceleration voltage of 30 kV, utilizing a Nova 600 NanoLab from FEI (the Netherlands). Before each Si layer deposition, the (100) silicon wafers were cleaned by the following steps: 10 s dip in 5% hydrofluoric acid (HF), 5 min wash in deionized (DI) water, 5 min etch in hot $H_2SO_4$:$H_2O_2$ 3:1, 5 min DI wash, 10 s dip in 5% HF, and 5 min DI wash. The Si layers were grown from a disilane ($Si_2H_6$) precursor, at a pressure of 2600 Pa and a temperature of 635 °C, using an Epsilon 2000 single wafer epitaxy tool from ASM International N.V. (the Netherlands). During the wafer loading procedure, the wafers were exposed to temperature steps of 850 °C for 13 s, followed by 725 °C for 120 s. After the final implantation, the wafers were treated with a rapid thermal anneal in an argon atmosphere at 650 °C for 30 s. The structures were formed by a final etch in KOH. First, a 3 s dip in 5% HF was done to remove the native silicon oxide and then the wafers were etched in 30% KOH at 36 °C for 4 to 8 min, depending on the targeted under-etch. Finally, the wafers were washed in DI water for 3 min and dried with $N_2$. The AFM measurements were made with an MFP-3D from Asylum Research (USA), and TEM images with a Tecnai G2 F20XT from FEI (the Netherlands).

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